to peak) at 1 kHz and V_{S_2} = 40 mV (peak to peak) at 1 kHz for the differential amplifier shown in figure 2. Assume the transistor is made of silicon with h_{ie} = 3.2 kΩ.

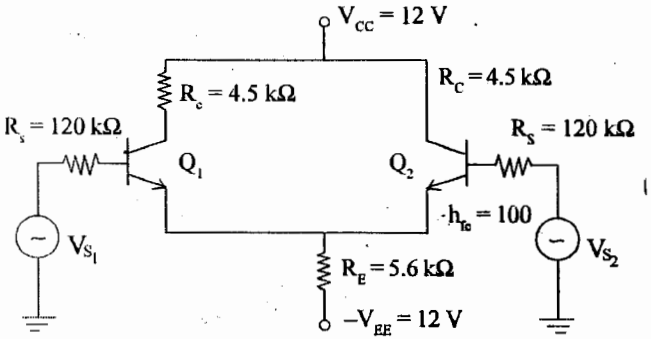

Figure 2

(c) Explain the operation of differential MOS pair :

(i) When common-mode input voltage

(ii) When a differential input voltage.

5. Attempt any *two* parts of the following : **(10×2=20)**

(a) Sketch the block diagrams of negative feedback arrangements. Derive an expression for gain with negative feedback.

(b) Show that the gain bandwidth product of an amplifier with negative feedback is the same as that of an ampl[illegible] without feedback.

(c) Draw the circuit of phase-shift oscillator and explain its working. State the advantage and disadvantages of this oscillator.

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0321 **Roll No.**

B. Tech.

(SEM. IV) THEORY EXAMINATION 2011-12

ELECTRONIC CIRCUITS

Time : 3 Hours *Total Marks : 100*

Note : Attempt ***all*** questions. Each question carries equal marks.

1. Attempt any ***four*** parts of the following : **(5×4=20)**

(a) Sketch an op-amp noninverting amplifier circuit. Explain the operation of the noninverting amplifier and derive an equation for its voltage gain.

(b) Explain common mode voltage, common mode voltage gain and common mode rejection ratio for operational amplifiers.

(c) Write equations for input impedance, output impedance and voltage gain for the noninverting amplifier.

(d) Sketch the circuit of a three input inverting summing amplifier. Explain the operation of the circuit and derive an equation for the output voltage.

(e) Explain the characteristics of ideal operational amplifier. What is the concept of virtual ground in op-amp ?

(f) Sketch an op-amp difference amplifier circuit. Explain the operation of the circuit and derive an equation for the output voltage.

2. Attempt any ***four*** parts of the following : **(5×4=20)**

(a) Explain the constructional detail of a MOSFET.

(b) Explain the enhancement type n MOSFET with suitable diagram.

(c) The FET is used as a voltage variable resistance. Give explanation.

(d) Draw and explain V-I characteristic of n-type depletion MOSFET.

(e) The amplifier of figure 1 utilizes an n-channel FET for which $V_P = -2.0$ V, $g_{mo} = 1.60$ mA/V and $I_{DSS} = 1.65$ mA. It is desired to bias the circuit at $I_D = 0.8$ mA using $V_{DD} = 24$ V. Assume $r_d >> R_d$, find (i) V_{GS}, (ii) g_m, (iii) R_S.

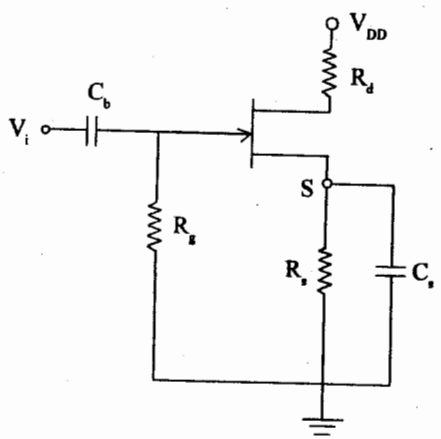

Figure 1

(f) Draw the circuit of CS amplifier of MOSFET with the help of small signal equivalent circuit and find out the expression for voltage gain and output impedance.

3. Attempt any ***two*** parts of the following : **(10×2=20)**

(a) (i) Sketch a family of CB output characteristics for a transistor. Indicate the active, cutoff and saturation regions.

(ii) What is meant by load line of a transistor ? Explain with a simple circuit diagram consisting of an NPN transistor.

(b) Why is potential divider biasing preferred over all other biasing circuit ? A CE amplifier employing an NPN transistor has load resistor RC connected between collector and V_{CC} supply of +16 V. For biasing a register R_1 is connected between collector and base. Resistor $R_2 = 30$ kΩ is connected between base and ground and resistor $R_E = 1$ kΩ is connected between emitter and ground. Draw the circuit diagram. Calculate the values of R_1 and R_C if $V_{BE} = 0.2$ V, $I_E = 2$ mA, $\alpha_o = 0.985$ and $V_{CE} = 6$ V.

(c) Draw the circuit of an RC coupled amplifier. Draw its gain V/s frequency characteristics and indicate cut-off frequency and bandwidth.

4. Attempt any ***two*** parts of the following : **(10×2=20)**

(a) What is the differential amplifier ? Explain the working with suitable diagram. Why matched transistors are required in a differential amplifier ?

(b) Calculate the operating point values, differential gain, common mode gain, CMRR, output if $V_{S_1} = 60$ mV (peak